Remarks

In the Office action of May 27, 2004, claims 1-22 (all pending claims) were rejected under 35 U.S.C. § 102(b) as being anticipated by Wenniger (U.S. Pat. No. 6,018,785).

Wenniger describes an apparatus having a resource accessible by a plurality of processes through first and second ports, wherein only one process can access the resource at any one time, a hardware semaphore that stores a value indicating the availability of the resource, and an interrupt circuit connected to the hardware semaphore and the plurality of processes that generates an interrupt in response to a change in the semaphore value. By generating a hardware interrupt when a shared resource becomes available, devices or processes that require access to the resource need not repeatedly poll the hardware semaphore. In these very general aspects it can be seen that Wenniger's apparatus is related to applicant's claimed multiprocessor system. However, the detailed technical features of the present invention differ in significant ways from that of Wenniger. Applicant amends the claim set to particularly point out the distinguishing features of the invention.

Wenniger's circuit is constructed with an arbitration unit (124, 244) to handle two competing requesting processes accessing the semaphore through respective left and right ports. In the present invention, the hardware semaphore is accessed via a system bus in which only one bus transaction can take place in any one clock cycle. (The bus system in the present invention effectively serializes access to the semaphore from multiple contenders.) There is no need for arbitrated access to the semaphore in applicant's invention. Rather, all that the semaphore hardware of the present invention needs to do is ensure that the semaphore's current value is read and thus, in the same clock cycle, changed to 1 (the claimed "second state") so as to indicate that the

semaphore has been acquired. Semaphore acquisition is just an atomic read-modify-write operation. Wenniger's arbitration unit (124; 244) with its cross-coupled NOR gates (134, 136; 234, 236) is unnecessary in applicant's system and the rest of the hardware semaphore becomes much simpler without the need for separate request and grant latches or edge detection logic. The combination of elements recited in applicant's claim 23 is neither taught nor suggested by Wenniger's semaphore structure. More particularly, the interrupt generation circuit of the present invention is much simpler (see, e.g., claims 26 and 27); instead of edge detection logic, semaphore interrupt cells (230a in Fig. 3) merely AND (gate 370) a flip-flop's (380) output (383) with a write signal (223) from the semaphore cell, and if the result (365) is a 1, we latch the output into an interrupt flip-flop (350). Otherwise, the current value (Q) of the interrupt flip-flop is latched into itself (303).

Another different is that Wenniger's processor contenders always write to the semaphore, both when attempting to obtain ownership of the resource (0 written to the left or right request latch) and also when releasing the resource (1 written to the left or right request latch). (See Wenniger's Tables 1 and 2). Wenniger's processors must perform an additional read of a grant register (G_L or G_R) following the write to a request latch (R_L or R_R). In the present invention (see method claim 28), a processor attempting to access the shared resource reads the semaphore cell and the data read gives the status of the attempt. The semaphore cell (220 in Fig. 3) contains a flip-flop (330) plus additional logic so that during a read bus transaction: (i) if the flip-flop's state is 0 (shared resource is available), then 0 is returned as read data and the flip-flop automatically toggles to a 1 state in the same clock cycle, but (ii) if the flip-flop's state is 1 (shared resource is unavailable), then 1 is returned as read data and the flip-flop remains unchanged in

its 1 state. The logical construction of this semaphore cell is set forth in claim 26. (See Fig. 3, element 220a) Likewise, claim 27 sets forth detailed structure of the semaphore interrupt cell (see Fig. 3, element 230a), so that as long as the semaphore cell's output remains 1, the output flip-flop (350) feeds back on itself, but when the semaphore cell changes to a 0, the output flip-flop is set to a 1 then cleared to 0 one clock cycle later. These actions and the structures associated with them are clearly not taught by Wenniger.

Applicant requests reconsideration of the application in light of the amended claims presented herein. A Notice of Allowance is earnestly solicited.

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

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